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PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/632,186	Filing Date:	July 30, 2003
Confirmation No.:	3961		
First Named Inventor:	Yi Ding		
Assignee:	ProMOS Technologies, Inc.		
Examiner:	Nguyen, Thanh T.	Art Unit:	2813
Attorney Docket No.:	M-15241 US		

San Jose, California
October 12, 2004

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR § 1.97(C)

Dear Sir:

Pursuant to 37 CFR § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying form PTO-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed except for United States Patent and United States Published Patent Applications.

Citation of these documents shall not be construed as:

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2. a representation that a search has been made, other than as described above; or

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Respectfully submitted,

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U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No.	Serial No.
	M-15241 US	10/632,186
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s)	
(Use several sheets if necessary)	Yi Ding	
	Filing Date	Group
	July 30, 2003	2813

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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,265,739	Jul. 2001	Yaegashi et al.			
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	AM	6,355,524	Mar. 2002	Tuan et al.			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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	AL	Shirota, Riichiro "A Review of 256Mbit NAND Flash Memories and NAND Flash Future Trend," February 2000, Nonvolatile Memory Workshop in Monterey, California, pages 22-31.
	AM	Naruke, K.; Yamada, S.; Obi, E.; Taguchi, S.; and Wada, M. "A New Flash-Erase EEPROM Cell with A Sidewall Select-Gate On Its Source Side," 1989 IEEE, pages 604-606.
	AN	Wu, A.T.; Chan T.Y.; Ko, P.K.; and Hu, C. "A Novel High-Speed, 5-Volt Programming EPROM Structure With Source-Side Injection," 1986 IEEE, 584-587.
	AO	Mizutani, Yoshihisa; and Makita, Koji "A New EPROM Cell With A Sidewall Floating Gate Fro High-Density and High Performance Device," 1985 IEEE, 635-638.
	AP	Ma, Y.; Pang, C.S.; Pathak, J.; Tsao, S.C.; Chang, C.F.; Yamauchi, Y.; Yoshimi, M. "A Novel High Density Contactless Flash Memory Array Using Split-Gate Source-Side-Injection Cell for 5V-Only Applications," 1994 Symposium on VLSI Technology Digest of Technical Papers, pages 49-50.
	AQ	Mih, Rebecca et al. "0.18um Modular Triple Self-Aligned Embedded Split-Gate Flash Memory," 2000 Symposium on VLSI Technology Digest of Technical Papers, pages 120-121.
	AR	Ma, Yale et al., "A Dual-Bit Split-Gate EEPROM (DSG) Cell in Contactless Array for Single Vcc High Density Flash Memories," 1994 IEEE, 3.5.1-3.5.4.

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	BC	6,414,872	2 Jul. 2002	Bergemont et al.			

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	BI	
	BJ	

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		OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)
	AA	United States Patent Application No. 10/440,466, entitled "Fabrication Of Conductive Gates For Nonvolatile Memories From Layers With Protruding Portions," Filed on May 16, 2003; Attorney Docket No.: M-12979 US.
	AB	United States Patent Application No. 10/440,005, entitled "Fabrication of Dielectric On A Gate Surface To Insulate The Gate From Another Element Of An Integrated Circuit," Filed on May 16, 2003; Attorney Docket No.: M-15203 US.
	AC	United States Patent Application No. 10/440,508, entitled "Fabrication Of Gate Dielectric In Nonvolatile Memories Having Select, Floating And Control Gates," Filed on May 16, 2003; Attorney Docket No.: M-15204 US.
	AD	United States Patent Application No. 10/440,500, entitled "Integrated Circuits With Openings that Allow Electrical Contact To Conductive Features Having Self-Aligned Edges," Filed on May 16, 2003; Attorney Docket No.: M-15205 US.
	AE	United States Patent Application No. 10/393,212, entitled "Nonvolatile Memories And Methods Of Fabrication," Filed on March 19, 2003; Attorney Docket No.: M-12902 US.
	AF	United States Patent Application No. 10/411,813, entitled "Nonvolatile Memories With A Floating Gate Having An Upward Protrusion," Filed on April 10, 2003; Attorney Docket No.: M-12903 US.
	AG	United States Patent Application No. 10/393,202, entitled "Fabrication of Integrated Circuit Elements In Structures With Protruding Features," Filed on March 19, 2003; Attorney Docket No.: M-15151 US.
	AH	United States Patent Application No. 10/631,941, entitled "Nonvolatile Memory Cell With Multiple Floating Gates Formed After The Select Gate," Filed on July 30, 2003; Attorney Docket No.: M-15171 US.
	AI	United States Patent Application No. 10/632,155, entitled "Nonvolatile Memory Cells With Buried Channel Transistors," Filed on July 30, 2003; Attorney Docket No.: M-15222 US.
	AJ	United States Patent Application No. 10/632,007, entitled "Arrays Of Nonvolatile Memory Cells Wherin Each Cell Has Two Conductive Floating Gates," Filed on July 30, 2003; Attorney Docket No.: M-15223 US.
	AK	United States Patent Application No. 10/631,452, entitled "Fabrication Of Dielectric For A Nonvolatile Memory Cell Having Multiple Floating Gates," Filed on July 30, 2003; Attorney Docket No.: M-15229 US.
	AL	United States Patent Application No. 10/632,154, entitled "Fabrication Of Gate Dielectric In Nonvolatile Memories In Which A Memory Cell Has Multiple Floating Gates," Filed on July 30, 2003; Attorney Docket No.: M-15230 US.
	AM	United States Patent Application No. 10/631,552, entitled "Nonvolatile Memories And Methods Of Fabrication," Filed on July 30, 2003; Attorney Docket No.: M-12902-1P US.
	AN	

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	AB	2003/0218908 A1	27 Nov. 2003	Park et al.			
	AC	2004/0004863 A1	8 Jan. 2004	Wang			
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	AG						
	AH						

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							Translation	
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	AI	EP 0 938 098 A2	25 Aug. 1999	Europe				
	AJ							
	AK							
	AL							

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	AM	United States Patent Application No. 10/798,475, entitled "Fabrication of Conductive Lines Interconnecting Conductive Gates in Nonvolatile Memories and Non-Volatile Memory Structures," Filed on March 10, 2004; Attorney Docket No. M-15296 US.
	AN	United States Patent Application No. 10/797,972, entitled "Fabrication of Conductive Lines Interconnecting First Conductive Gates in Nonvolatile Memories Having Second Conductive Gates Provided By Conductive Gates Lines, Wherein The Adjacent Conductive Gate Lines For The Adjacent Columns Are Spaced From Each Other, And Non-Volatile Memory Structures," Filed on March 10, 2004: Attorney Docket No. M-15297 US.
	AO	
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